REMARKS

Claims 1-51 are pending in the present application. Claims 32-51 have been withdrawn from consideration; and claims 1 and 22 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, Applicant's election without traverse of Group 1 claims (i.e., claims 1-31); claims 1-10 and 15-31 were rejected under 35 U.S.C. Section 102(b) as anticipated by U.S. Patent No. 5,675,170 (Kim et al.); and claims 1, 7 and 11-14 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,642,667 (Magee).

35 U.S.C. Section 102 Rejections

Claims 1-10 and 15-31 were rejected under 35 U.S.C. Section 102(b) as anticipated by Kim et al. Applicant respectfully traverses the rejection.

Claims 1 and 22 have been amended to clarify the invention. In particular, claims 1 and 22 have been amended to recite: "an injections site associated with said CMOS semiconductor structure." Support for the amendment is provided at least at paragraph 4 and pargraph 8 of the specification. Therefore, it is respectfully submitted that the amendments raise no question of new matter.

Kim et al. discloses an apparatus for decreasing latch-up in I/O circuits such as a data output buffer.[1] In particular, Kim et al. discloses an N-well guard ring 4 that is disposed under a data input and output pad 5.[2] In addition, Kim et al. discloses the N-well guard ring 4 is not only formed on a portion adjacent to the P-well 2 and the N-well 3, but also *formed on a portion of the P-type substrate under the data output pad* 5, wherein the guard ring 4 is formed as a single enlarged N-well guard ring (emphasis added).[3]

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[1] Kim et al. ABSTRACT.
[2] *Id.* at FIG. 3, FIG. 4, column 2, lines 51-53.
[3] *Id.* at FIG. 3, FIG. 4, column 2, lines 53-56.

Further, Kim et al. discloses the N-well guard ring 4 that does not have a separated structure such as the first and the second N-well guard ring **4A** and **4B** in CMOS technologies, but instead has a widely expanded and integrated structure.[4] Moreover, Kim et al. discloses that the minority carriers transmitted from the second N^+ region **23** to the first N^+ pickup region **34** of the PMOS transistor are completely captured by the expanded N-well guard ring **4**, thereby preventing generation of the latch-up in NMOS and PMOS technologies.[5]

However, Kim et al. nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; an injection site associated with said *CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

In addition, claim 22 recites similar language. That is, in contrast to Kim et al., the claimed invention is directed toward a modern CMOS semiconductor structure.

Further, though Kim et al. discloses an apparatus that decreases latch-up in NMOS and PMOS technologies, it is respectfully submitted that Kim et al. does *not* disclose an apparatus with the CMOS semiconductor structure of the claimed invention and that is applicable to modern CMOS technologies. As specifically discussed above, Kim et al. requires the use of the area under the I/O pad for expanding the N-well guard ring to prevent latch-up. In contrast to Kim et al., in the claimed invention and modern CMOS technologies the area under I/O pads is *not* available because additional circuits are placed under the I/O pads due to restraints on integrated circuit area and requirements for increased integrated circuit functionality. Due to these restraints and requirements, the apparatus for latch-up prevention in Kim et al. is not applicable to more modern CMOS technologies. Thus, Kim et al. does not disclose the "CMOS semiconductor structure" of the claimed invention and modern CMOS technologies.

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[4] *Id.* at FIG. 1, FIG. 2, column 2, lines 58-61.
[5] *Id.* at column 2, lines 61-65.

Further, the structure/approach disclosed by Kim et al. of expanding the N-well guard ring to collect injected minority carriers to reduce latch-up is *not applicable* for non-standard latch-up tests "arising from a cable discharge event," as recited in claims 19 and 29. That is, the structure/approach of Kim et al. is not applicable for these tests because the current injected during the recited "cable discharge event" would require an unreasonably large N-Well guard ring in the apparatus of Kim et al. in order to prevent latch-up. Moreover, the expanded/large N-Well guard rings of Kim et al. would be very difficut to implement in a modern CMOS semiconductor structure because these large/expanded guard rings would increase the size of I/O cells of the integrated circuit and would result in a larger requirement for integrated circuit area for these cells and thus reduce integrated circuit functionality.

Therefore, at least for the reasons above, it is respectfully submitted that Kim et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 1 and 22, and claims dependent thereon patentably distinguish thereover.

Claims 1, 7 and 11-14 were rejected under 35 U.S.C. 102(b) as being anticipated by Magee. Applicant respectfully traverses the rejection.

Magee discloses a bipolar lateral transistor that was compatible with "current NMOS or CMOS processing."[6] It should be noted that "current" at the time of the Magee patent disclosure was 1987. In particular, Magee discloses an npn lateral transistor structure that is formed in a very lightly doped p^- -type silicon substrate **11**.[7] In addition, Magee discloses a lightly doped n^- -type well **12** that is deeply diffused into the substrate **11** and a further lightly doped p^- -type well **13** that is diffused into the n^- -type well **12**.[8] Further, Magee discloses a p-type region **14** that is diffused to form the intrinsic base, together with a p^+ -type region to act as a base contact.[9] Furthermore, Magee discloses that N^+ regions are added for the emitter **16** and collector contact region **17**, during which the emitter is diffused through the same window as the base **14**, to end up with a narrow P region surrounding and self aligned to the emitter. Moreover, Magee

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[6] Magee at ABSTRACT and column 2, lines 29-35.
[7] Magee at column 1, lines 62-64.
[8] Magee at column 1, lines 64-66.

discloses the contact region 17 provides a collector for lateral transistor action and a collector contact for vertical transistor action.[10]

However, Magee nowhere discloses, as recited in independent claim 1:

> [a] *CMOS semiconductor structure* comprising: a substrate; a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; an injection site associated with said *CMOS semiconductor structure;* and a plurality of contact regions inter-spaced a varying distance between said circuit structures (emphasis added).

That is, in contrast to the Magee patent issued in 1987, the claimed invention is directed toward modern "CMOS semiconductor structures," as recited in claim 1. It is respectfully submitted that the apparatus and structure of Magee is not applicable to modern CMOS semiconductor structures that have restraints on integrated circuit area and requirements for increased integrated circuit functionality.

Further, Magee was directed toward building bipolar transistors in the current CMOS processes of 1987. However, Magee was not directed toward the problem of reducing latch-up in modern CMOS technologies or in the "CMOS semiconductor structures," as recited in claim 1.

Moreover, Magee discloses an arrangement of n+ and p+ taps that is not feasible in due to space constraints in modern CMOS technologies.[11] Thus, it is respectfully submitted that Magee teaches away from the claimed invention.

Therefore, at least for the reasons above, it is respectfully submitted that Magee does not disclose, anticipate or inherently teach the claimed invention and that claim 1, and claims

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[9] Magee at column 1, lines 66-68.
[10] Magee at column 2, lines 5-7.
[11] *Id.* at FIG. 2.

dependent thereon patentably distinguish thereover.

Conclusion

Based on the above amendments and arguments, Applicant respectfully submits that the application is in condition for allowance. Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 50-3223, under Order No. 21806-00156-US, from which the undersigned is authorized to draw.

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Respectfully submitted,

By Myron K. Wyche
Myron K. Wyche, Reg. No. 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant